

WHAT IS CLAIMED IS:

1. A system for allowing conventional memory test circuitry

2 to test parallel memory arrays, comprising:

3 bit pattern distribution circuitry that causes a probe bit
4 pattern generated by said memory test circuitry to be written to
5 each of said memory arrays;

6 a pseudo-memory, coupled to said bit pattern distribution
7 circuitry, that receives a portion of said probe bit pattern; and

8 combinatorial logic, coupled to said pseudo-memory, that
9 employs said portion and data-out bit patterns read from said
10 memory arrays to generate a response bit pattern that matches said
11 probe bit pattern only if all of said data-out bit patterns match
12 said probe bit pattern.

2. The system as recited in Claim 1 wherein said bit pattern

2 distribution circuitry comprises a multiplexer coupled to said each
3 of said RAM arrays.

3. The system as recited in Claim 1 wherein portion is a

2 single bit.

4. The system as recited in Claim 1 wherein said
2 combinatorial logic comprises comparator circuitry that produces a
3 zero bit only if all of said data-out bit patterns match said probe
4 bit pattern.

5. The system as recited in Claim 4 wherein said
2 combinatorial logic further comprises corrector circuitry that
3 produces said response bit pattern that matches said probe bit
4 pattern only if said comparator circuitry produces said zero bit.

6. The system as recited in Claim 1 wherein said response
2 bit pattern differs from said probe bit pattern by a single bit if
3 at least one of said data-out bit patterns fails to match said
4 probe bit pattern.

7. The system as recited in Claim 1 wherein a portion of
2 said response bit pattern matches a corresponding portion of a
3 data-out bit pattern from one of said memory arrays.

8. A method for allowing conventional memory test circuitry

2 to test parallel memory arrays, comprising:

3 causing a probe bit pattern generated by said memory test
4 circuitry to be written to each of said memory arrays;

5 receiving a portion of said probe bit pattern into a pseudo-
6 memory; and

7 employing said portion and data-out bit patterns read from
8 said memory arrays to generate a response bit pattern that matches
9 said probe bit pattern only if all of said data-out bit patterns
10 match said probe bit pattern.

9. The method as recited in Claim 8 wherein said causing

2 comprises sending a signal to a multiplexer coupled to said each of
3 said RAM arrays.

10. The method as recited in Claim 8 wherein said portion is

2 a single bit.

11. The method as recited in Claim 8 wherein said employing

2 comprises producing a zero bit only if all of said data-out bit
3 patterns match said probe bit pattern.

12. The method as recited in Claim 11 wherein said employing
2 further comprises producing said response bit pattern that matches
3 said probe bit pattern only if said zero bit is produced.

13. The method as recited in Claim 8 wherein said response
2 bit pattern differs from said probe bit pattern by a single bit if
3 at least one of said data-out bit patterns fails to match said
4 probe bit pattern.

14. The method as recited in Claim 8 wherein a portion of
2 said response bit pattern matches a corresponding portion of a
3 data-out bit pattern from one of said memory arrays.

15. An integrated circuit, comprising:

2 a processor;

3 a plurality of identical memory arrays under control of said

4 processor;

5 conventional built-in test (BIST) circuitry;

6 multiplexers, associated with said plurality of identical

7 memory arrays and coupled to said processor and said conventional

8 BIST circuitry, that allows said conventional BIST circuitry to

9 take said control from said processor; and

10 a system that allows said conventional BIST circuitry to test

11 said plurality of identical memory arrays in parallel, including:

12 bit pattern distribution circuitry that causes a probe

13 bit pattern generated by said conventional BIST circuitry to

14 be written to each of said plurality of memory arrays,

15 a pseudo-memory, coupled to said probe bit pattern

16 distribution circuitry, that receives a portion of said probe

17 bit pattern, and

18 combinatorial logic, coupled to said pseudo-memory, that

19 employs said portion and data-out bit patterns read from said

20 plurality of memory arrays to generate a response bit pattern

21 that matches said probe bit pattern only if all of said data-

22 out bit patterns match said probe bit pattern.

16. The integrated circuit as recited in Claim 15 wherein
2 said portion is a single bit.

17. The integrated circuit as recited in Claim 15 wherein
2 said combinatorial logic comprises comparator circuitry that
3 produces a zero bit only if all of said data-out bit patterns
4 match said probe bit pattern.

18. The integrated circuit as recited in Claim 17 wherein
2 said combinatorial logic further comprises corrector circuitry that
3 produces said response bit pattern that matches said probe bit
4 pattern only if said comparator circuitry produces said zero bit.

19. The integrated circuit as recited in Claim 15 wherein
2 said response bit pattern differs from said probe bit pattern by a
3 single bit if at least one of said data-out bit patterns fails to
4 match said probe bit pattern.

20. The integrated circuit as recited in Claim 15 wherein a
2 portion of said response bit pattern matches a corresponding
3 portion of a data-out bit pattern from one of said memory arrays.